Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.015”**

**.015”**



**40**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .0024” X .0024”**

**Backside Potential: COLLECTOR**

**Mask Ref: 40**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 2/7/23**

**MFG: FAIRCHILD / ON SEMI THICKNESS .008” P/N: 2N2857**

**DG 10.1.2**

#### Rev B, 7/1